## Remarks

Reconsideration of the application is requested. Applicants appreciate the allowance of claims 1-23 and allowability of claims 32, 33, 36, and 37. However, applicants respectfully traverse the rejection of certain claims as anticipated by Momtaz and other claims as unpatentable over Momtaz in view of Anderson and Aung.

**The § 102(b) Rejections**

Claim 24 is directed to a deserializer. It recites, among other things:

> sync detect logic coupled to the clock divider and operable to assert a parallel clock enabling signal that enables the clock divider to generate the divided clock signal, the sync detect logic including a reloadable register operable to store a programmable synchronization bit pattern associated with a communications protocol and a bit pattern comparator operable to compare the stored programmable synchronization bit pattern with a synchronization bit pattern within the recovered serial data bits and to assert or not assert the parallel clock enabling signal as a result of the comparison

Through this programmable feature, the sync detect logic can assert a variable parallel clock enabling signal that controls the clock divider, effectively making the divider's output clock frequency (RPCLK) programmably variable. This, in turn, makes the deserializer's serial-to-parallel shift register programmably variable, enabling it to handle data of multiple protocols with transmission characters have different numbers of bits (e.g., 12 bits for 10B/12B Serial Data and 10 bits for 8B/10B Fibre Channel Serial Data). For further details of an embodiment of the invention, see application Figs. 18 and 19; page 36, line 5 to page 37, line 5; page 37, line 18 to page 38, line 18; and page 40, line 4 to page 42, line 8.

Similar limitations in structure and method are recited in independent claims 31 and 34.

Momtaz does not teach or suggest this approach. Rather, as described in the patent, Momtaz discloses a conventional deserializer that is clocked at a fixed frequency (106.5 MHz) to accommodate data of a single protocol (Fibre Channel at 1.0625 GHz):

> Synchronized serial data is then directed to a deserializer and byte synk circuit 38 which restores 10-bit parallel data transmission characters from the high speed serial bit stream. In conventional fashion, the deserializer and byte synk circuit 38 further recovers two 53.125 MHz receiver byte clocks (not shown) which are 180º out-of-phase with one another and ultimately used by follow-on circuitry to clock the 10-bit parallel output data.

Col. 8, lines 13-21; Fig. 2.

There is nothing in Momtaz describing or suggesting that the frequency of these byte clocks can somehow be varied to enable deserializer 38 to accommodate data of other protocols, such as 12-bit 10B/12B serial data.

In the action the Examiner points to three sections of Momtaz (col. 4, lines 4-14; col. 8, lines 20-31; and col. 8. lines 32-51) as disclosing the claimed programmable feature. Applicants respectfully disagree. The first section describes the function of a LCKREF signal for switching the detection mode of the phase lock loop. It states nothing about changing the frequency of the clock signal applied to the deserializer to accommodate data of different protocols. The second section merely describes how the applied clock signal is aligned properly with the data being received by the deserializer. Again, it states nothing about changing the frequency of the applied clock signal. The third section describes how the PLL is used to recover a synchronization clock signal from the incoming serial data stream. Again, it states nothing about changing the frequency of the clock signal applied to the deserializer.

Momtaz cannot thus be said to anticipate the claimed inventions, for at least the reason that it does not disclose the above-described programmable feature.

**The § 103(a) Rejections**

As noted above, Momtaz (the primary reference for this rejection) advocates the conventional approach of providing a clock with a fixed frequency for deserializing recovered serial bits. By advocating this approach, Momtaz cannot be said to teach or suggest what is claimed. The same is true for Anderson and Aung, which add nothing to Momtaz in this respect.

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For the reasons stated above, applicants submit that none of the claims are anticipated by the prior art and that the prior art does not establish a prima facie case of their obviousness. Applicants therefore believe that the present claims are in now in condition for allowance, and such action is respectfully requested.

Please call the undersigned if he can be of any assistance in this case.

Respectfully submitted,

Date: 6/9/05 By _____

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